# Evaluation of the Xilinx™ ML505/XUPV5 Platform for EECS150

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## Introduction

## This document is an evaluation of the Xilinx™ ML505/XUPV5 as a possible replacement of the CaLinx2+ board for EECS150 use starting Spring 2009. To summarize, the Xilinx™ board is well-suited for EECS150, seeing that “glue logic” and firmware are at the heart of this course. The Xilinx™ platform can be used to teach design of small, efficient interfaces, which are the cornerstone of modern digital logic design. The ML505/XUPV5 is an excellent upgrade for the CaLinx2+, as it matches and builds on the IO offered by the CaLinx2+, while providing a large, high-performance modern FPGA.

## Details

### Large, Modern FPGA: Xilinx™ Virtex5 XC5VLX50T (XC5VLX110T)

With 29K (70K for the 110 part) 6-input LUTs, and over 2Mbits on-chip RAM, the FPGA in question (a high-end Xilinx™ FPGA which performs at up to 500MHz both as advertised and measured at Berkeley) greatly exceeds the capabilities of the XCV2000E on the CaLinx2+.

### Simple On-Board IO (GPIO)

The Xilinx™ platform features 15 LEDs, 8 DIP switches, and 5 pushbuttons comparable to the CaLinx2+ (8 LEDs, 8 pushbuttons, 16 DIP switches). A rotary switch, a new simple interface, is also present. The loss of the 7-segment displays on the CaLinx2+ board is of little concern with the advent of the 16 × 2 LCD on both boards.

### Expansion Connectors (Expandability and Suggested Expansion Board Features)

The Xilinx™ platform offers 64 high-speed single-ended IO (32 can be used as 16 differential pairs) for expansion or logic analyzer access. The power and layout of the connectors are well-suited for addition of a daughter board, in contrast to most FPGA boards, including the CaLinx2+. The ML505/XUPV5 offers more than enough IO to implement additional features such as Bluetooth and ZigBee radio, additional LEDs and switches, game controllers, etc. with enough left over for logic analyzer use.

### Advanced (Network/Multimedia/High-Speed) On-Board IO and Other Peripherals

The Xilinx™ platform features a rich set of on-board peripherals including audio IO, video IO, a 1000/100/10 Ethernet PHY, along with various high-speed interfaces. Although the board does not offer quad Ethernet, the Gigabit PHY delivers more than 4 times the performance and is a potent replacement. The board offers a rich, diverse set of interesting IO, which is of utmost importance to the EECS150 curriculum. A shortcoming of the board is the fact that only DDR2 DRAM is offered, a difficult interface to implement; nonetheless, it is a universal interface, giving students the experience. The only IO left to be desired are radio, an easy addition in the form of a daughter board.

Overall the peripherals offered by the ML505/XUPV5 greatly exceed those on the CaLinx2+, while preserving hardware-friendly interfaces, which are essential to EECS150.

### Physical Characteristics: Quality of Construction, Fragility, and Jumper Settings

Due to detachable and fragile elements and dangerous jumper settings, the Xilinx™ platform is in need of Plexiglas before it can be used in the EECS150 environment. Also, even though the board comes with mounting holes for a fan, no cooling solution of any kind is provided with the board at present. Given the two are provided, the board is well-organized, compact, and has well-placed connectors making it well suited to the lab environment.

### CAD Tools

The CAD tool flow used by EECS150 in the recent semesters (ISE, ModelSim, SynplifyPro, Chipscope) has been proven effective if at times frustrating. Experienced users are readily available, resulting in a fast learning curve for new students and TAs. Synthesis and PAR times for the FPGA in question are comparable to the XCV2000E on the CaLinx2+, rendering the CAD tools equivalent to those used for the CaLinx2+. The annoyances associated with the CAD tools are essentially independent of the board used, and the suite provided for both of these boards is continuously improving.

### Availability of Boards

A question to be considered is the physical availability of the XUPV5. The ML505, however, can easily be purchased, though a donation is possible. Boards are, therefore, available on demand, with replacements likely to be available for a long time. The similarity of the two boards, coupled with the presence of programming cables in 125 Cory renders the two boards more or less equivalent based on the information given to us regarding the XUPV5.

### Support and Availability of Expertise

Since the design techniques and CAD tools for the Xilinx™ platform in question coincide with those for the CaLinx2+, there is a large body of code and expertise readily transferable to the Virtex5 platform. The RAMP group already supports the ML505/XUPV5 board, meaning a higher standard for the code, documentation, and a higher quality of EECS150 overall. Finally, because the ML505 and XUPV5 are commercial Xilinx™ boards, and used by research as well, they will receive significant technical support from Xilinx™ for the foreseeable future. Commercial support is a benefit that has not been available with the CaLinx2+.

## Conclusion

Although the Xilinx™ ML505/XUPV5 has its shortcomings (heat sink and Plexiglas), it is well suited the EECS150 curriculum, and provides a superset of the educational opportunities, offered by the CaLinx2+ boards. The board offers a superset of the CaLinx2+ IO, including newer and more interesting interfaces, and extends it with a rich set of high-speed interfaces, while offering a more modern FPGA to students. The availability of a large number of diverse interfaces is vital for EECS150, and the ML505/XUPV5 provides just that. Strengthened by the availability of experienced users and high-quality support, this platform is an excellent replacement for the CaLinx2+.